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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/666,552	09/19/2003	Thomas R. Apel	TRQ-12893	5545

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EXAMINER	
SHINGLETON, MICHAEL B	

ART UNIT	PAPER NUMBER
2817	

DATE MAILED: 05/17/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/666,552	APEL ET AL.	
	Examiner	Art Unit	
	Michael B. Shingleton	2817	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *2-27-2006*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-22* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-22* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Michael B. Shingleton
MICHAEL B. SHINGLETON
PRIMARY EXAMINER
ART UNIT 2817

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

Claims 1, 3, 4, 6-11, 13, 14, 16, 17, 18, 20 and 21 are rejected under 35 U.S.C. 103(a) as being unpatentable over Otani US2001/0022534 A1 (Otani) in view of Holt of record.

Figure 2 and the relevant text of Otani discloses a power amplifier circuit and "method of amplifying an input signal" having the steps/structure of providing an input signal to a first amplifier 25 wherein the first amplifier receives an input signal as is clearly illustrated in Otani, introducing a first delay to the input signal via elements like L3, L4 as shown in Figure 2 of Otani whereby a delayed input signal is received by a second amplifier 26, introducing a second delay to the output signal of the first amplifier 25 called in some of the claims as the "first output signal" via elements like L5-L6 as is clearly illustrated in Figure 2 of Otani and combining the output signals with one of the output signals being the one that is delayed by the second delay and the other one being the one from the second amplifier 26. Note that this structure of Otani directly parallels the structure of the disclosed invention shown in Figure 3 of the instant application. In particular note that only one delay is in the input path to the amplifier 310B whereas there is only one delay in the output path formed in the leg of the circuit that does not include the amplifier 310B. The placement of one delay in the input of one leg and the placement of the other delay in the other leg of a two leg arrangement is what applicant is trying to describe by the amendment to claim 1 and 13 that recites "wherein the delayed input signal is delayed relative to the input signal received by the first amplifier". This amendment is what has necessitated this new ground of rejection. The second delay is called by applicant as an impedance inverter and is composed of elements 342 (capacitor), 341(inductor) and 343(capacitor). The capacitor C8, the inductor L7 and the capacitor C10 of Otani forms the same structure connected in the same manner as applicant's second delay or impedance inverter. Therefore because the structures are the same Otani is seen as having the function of an impedance inverter configured to provide impedance inversion and introduce a second delay to the first output signal.

With respect to claims 1 and 13 these claims recite the method/structure of providing first and second bias voltages to the two amplifiers via a bias means such that the first and second amplifiers operate in linear mode. Holt as noted in the previous office actions clearly teaches that it is well known to provide a bias circuit to an amplifier. Even though Otani fails to show a bias circuit a bias circuit is necessary in order for the device to work. Note that the description of an invention is such that one skilled in the art would have been able to make the invention of Otani. Holt in addition to showing that a bias circuit is a necessary part of an amplifier circuit, teaches that the level at which the bias is selected determines the class of operation. In particular Holt teaches that one of routine skill could select the bias so as to obtain linear operation. Linear operation is a measurement of how accurately the amplifier reproduces an input signal multiplied by a gain, ideally S_{out} is equal to S_{in} multiplied by a Gain. Linear operation produces the most accurate reproduction of the input signal over a range of values for the input signal.

Accordingly, it would have been obvious to one of ordinary skill in the art at the time the invention was made to have provided Otani with a bias arrangement(s) for the first and second amplifiers as a bias arrangement is necessary for the amplifier to work as taught by Holt and to select the bias point to be that of linear operation so as to produce the most accurate reproduction of the input signal over a range of values of the input signal as taught by Holt.

With respect to claim 3, the terminal "b" of Otani forms the output terminal as recited.

With respect to claims 4 and 18, the elements 21 and 22 form an impedance matching circuit.

With respect to claims 6 and 16, the structure of the first delay that includes capacitors C3 and C4 and the inductor L3 is the same structure as elements 332, 331 and 333 of the instant application and like that of the second delay this too would form an "impedance inverter circuit". Note the discussion of the impedance inverter circuit above.

With respect to claims 7 and 17, here the result effective variables are selected so that "the first amplifier exhibits a first impedance optimum load, and the second amplifier exhibits a second impedance optimum load, and the impedance inverter circuit exhibits a characteristic impedance to the first impedance". Note the word "optimum" used in the claims. The selection of the optimum values for the operation of a circuit has been long held to involve only routine skill in the art. As optimization involves merely routine skill, one of ordinary skill clearly would have found selecting the operating point of a circuit for optimum operation obvious. Thus it would have been obvious to one having ordinary skill in

the art at the time the invention was made to have selected the circuit values of Otani such that the optimum operation of having "the first amplifier exhibits a first impedance optimum load, and the second amplifier exhibits a second impedance optimum load, and the impedance inverter circuit exhibits a characteristic impedance to the first impedance" occurs, since it has been held that discovering an optimum value of a result effective variable involves only routine skill in the art. In re Boesch, 617 F.2d 272, 205 USPQ 215 (CCPA 1980).

With respect to claims 8 and 14, even though Otani appears to be silent on selecting the first delay to be equal to the second delay, in order for the output signal to be properly combined these two delays have to be equal. Thus Otani is seen as inherently having the first delay to be equal to the second delay.

With respect to the claimed subject matter that recites the sets of transistors for the various amplifiers. An amplifier formed of but a signal transistor can be formed from a plurality of transistors connected in parallel. Figure 3 of the instant application shows the use of a single transistor amplifier and Figures like Figure 4A of the instant applicant shows an amplifier that is formed from a plurality of parallel-connected amplifiers. The examiner does not see these as patentability distinct species for the use of a single amplifier or a plurality of parallel-connected transistors to form an amplifier are well known art recognized equivalents. In fact it is conventionally know that a plurality of parallel-connected amplifiers can handle more current than an amplifier of a single transistor where the single transistor is the same transistor structure of the transistors of the parallel arrangement. Thus it would have been obvious to one having ordinary skill in the art at the time the invention was made to replace the single transistor amplifier units of Otani with parallel connected transistors since the examiner takes Official Notice of the equivalence of the use of a single transistor and a parallel arrangement of transistors for their use in the amplifier art and the selection of any of these known equivalents to provide an amplifier function would be within the level of ordinary skill in the art. One of ordinary skill in the art would have been further motivated to replace the single transistor of the amplifier elements of Otani with ones that are composed of a plurality of parallel connected amplifier elements so as to allow for higher current operation as is conventionally known in the art. Note that the first and second bias voltages recited by the claims could be the same level and thus the necessary bias producing means mentioned above would provide the first and second bias voltages to the first and second amplifiers as claimed. Also note the claims must be given their broadest reasonable interpretation and the first amplifier can be composed of at least four parallel connected transistors as noted above. In this situation two of the transistors would be a

first subset (Note for example claim 11.) and the other two would be the "second subset" that is for receiving the second bias voltage (Note for example claim 11). Claim 21 of the instant application recites the same basic subject matter as claim 11 except in method form. Here in claim 21 the second subset would be the third set of transistors of the first amplifier.

Claims 2 and 15 are rejected under 35 U.S.C. 103(a) as being unpatentable over Otani and Holt as applied to claims 1, 3, 4, 6-11, 13, 14, 16, 17, 18, 20, and 21 above, and further in view of Cheng et al..

Otani as noted above is silent on the showing of the necessary bias generation means to be used with the various amplifiers of the arrangement. The addition of a bias means would have been obvious as noted as taught by Holt and described in the above rejection. In addition applicant claims subject matter that include means for activating the first bias voltage and deactivating the second bias voltage when a control signal identifies a low power mode and means for activating both the first and second bias voltages when the control signal identifies a high power mode (Note at least claim 2 of the instant application.). This subject matter is the disabling or enabling of the various legs of the amplifier arrangement via the bias generation means.

Cheng teaches that one can selectively supply the bias voltages to each of the parallel-connected amplifiers, i.e. each amplifier leg, so as to control the operation of these amplifiers, i.e. whether the amplifiers are on or they are off. This clearly controls the amount of power delivered to the load (See page "4" and in particular note paragraph "[0037]".

Thus it would have been obvious to one of ordinary skill in the art at the time the invention was made to have the bias control circuit of Otani in view of Holt selectively control the application of the bias voltage to the respective amplifiers with respect to a control signal so as to control the amount of power output as taught by Cheng.

Claims 5 and 19 are rejected under 35 U.S.C. 103(a) as being unpatentable over Otani and Holt as applied to claims 1, 3, 4, 6-11, 13, 14, 16, 17, 18, 20, and 21 above, and further in view of Sedra.

Each leg of the arrangement of Otani and Holt is composed of but a single stage amplifier arrangement. Note that Figures like Figure 3 of the instant application and the corresponding claims recite that each leg of the amplifier arrange can have a preamplifier stage or "input amplifier stage" like element 310 and a final amplifier stage like element 320. This does not present a patentable distinction over the prior art as it is common knowledge that multiple stage amplifiers are art recognized equivalents to a single stage amplifier and have advantages over the use of a multiple stage amplifier arrangement

over that of a single stage amplifier arrangement. One advantage is that the input stage can be made to have a high input resistance which is done to avoid signal loss. Another is that the first stage can provide large common-mode rejection while the intermediate and final stages can provide the bulk of the gain. Another advantage is that the final stage can provide a low impedance that can provide larger amounts of current. These and other advantages are described on page 749 of Sedra.

Thus it would have been obvious to one having ordinary skill in the art at the time the invention was made to have replaced the single stage amplifiers in the Otani and Holt combination with multiple stage amplifiers since the examiner takes Official Notice of the equivalence of the use of single stage amplifiers and multiple stage amplifiers for there use in the amplifier art and the selection of any of these known equivalents to form an amplifier function would be within the level of ordinary skill in the art. Furthermore one of ordinary skill in the art would have been motivated to make the combination for one of ordinary skill would have been motivated to utilize a multiple stage arrangement over a single stage arrangement for the decrease in signal loss, the large amount of common mode rejection that occurs with such an arrangement and the production of larger output current levels that are possible with such arrangements as taught by Sedra.

Claims 12 and 22 are rejected under 35 U.S.C. 103(a) as being unpatentable over Tani and Holt as applied to claims 1, 3, 4, 6-11, 13, 14, 16, 17, 18, 20 and 21 above, and further in view of Taniguchi et al. 5,162,756 (Taniguchi) of record).

With respect to claimed the subject matter that includes a third amplifier that is configured to receive an input signal. Thus this claimed subject matter is directed toward the species as represented by Figure 6 of the instant application. The examiner does not see a patentable distinction between a two-legged amplifier arrangement and a three or more legged amplifier arrangement. This parallels the providing of parallel-connected transistors to replace a single transistor for the more legs of an amplifier arrangement the more current the amplifier can handle and/or produce. Of course the more current means that the more power the amplifier arrangement can handle or produce. This is clearly apparent from Taniguchi and in particular note Figure 2 where four legs are provided thereby allows twice the amount of current handling as compared to a two-legged amplifier arrangement where all things are equal, i.e. the same amplifier units are used for the legs etc..

Thus it would have been obvious to one of ordinary skill in the art at the time the invention was made to add as many legs, i.e. legs like where the delay is introduced on the output signal of the leg, as one desires dependent on the required or desired current handling capabilities as taught by Taniguchi.

Response to Arguments

Applicant's arguments with respect to claims of record have been considered but are moot in view of the new ground(s) of rejection.

Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Michael B. Shingleton whose telephone number is (571) 272-1770.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Robert Pascal, can be reached on (571)272-1769. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306 and after July 15, 2005 the fax number will be 571-273-8300. Note that old fax number (703-872-9306) will be service until September 15, 2005.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

MBS
November 20, 2005
May 1, 2006

Michael B. Shingleton
PRIMARY EXAMINER